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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/967,036	09/28/2001	Clyde S. Clark	42390P12321	4845

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EXAMINER	
MASON, DONNA K	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 10/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/967,036	CLARK ET AL.	
	Examiner	Art Unit	
	Donna K. Mason	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *02 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,10-16 and 19-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,10-16 and 19-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 10-16 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claims contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention.

Claim 10, as amended recites, "a first storage device coupled with a first processor" in line 2, and recites, "a second storage device coupled with a second processor" in line 5. Although this subject matter is disclosed with regard to the prior art (*see e.g.*, Fig. 1, items 125 and 140), this feature was not disclosed with regard to the invention. For example, as shown in the embodiments, which disclose the present invention (Figs. 6-13), neither a first storage device nor a second storage device is shown. *Therefore, the Examiner has not considered the new matter in the examination of claims 10-16.*

Claims 11-16 inherit the deficiencies of independent claim 10.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 10-16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. Claim 10 recites "hardware associated with the first processor and the second processor to detect faults in the processors transfer control . . ." in lines 8-9. This language lacks clarity. It appears that "and to", or similar language, should be inserted between "processors" and "transfer" in line 9.

6. Claim 10 recites the limitation "the processors" in line 9. There is insufficient antecedent basis for this limitation in the claim. The examiner recommends changing "the processors" to --the first processor and the second processor--.

7. Claims 11-16 inherit the deficiencies of independent claim 10.

Claim Rejections - 35 USC § 102

8. Claims 1-7, 10-16, and 19-25 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,618,783 to Hammersley.

With regard to independent claims 1, 10, and 19, Hammersley discloses a method, system (Fig. 2, item 105), and a machine-readable medium (column 4, lines 55-57), where the method includes the steps of: operating a first processor (Fig. 2, item 110(a) connected with a first bus (Fig. 2, item 124(a)) and a second bus (Fig. 2, item 124(b)) wherein the first processor controls the first bus; operating a second processor (Fig. 2, item 110(b)) connected with the first bus and the second bus wherein the second processor controls the second bus; detecting faults via hardware associated

with the first processor and the second processor (column 6, lines 25-27; Fig. 2 items 120, 122, 134a and 134b; column 4, lines 64-67 to column 5, lines 1-3), where the hardware includes a Redundant Host Controller (column 5, lines 41-64); and responsive to an occurrence of a fault in the first processor, transferring control of the first bus to the second processor via hardware associated with the first processor and the second processor (column 6, lines 40-67 to column 7, lines 1-9).

With regard to claims 2-6, 11-15, and 20-24, Hammersley discloses the method, system, and machine-readable medium, where operating a first processor includes the steps of: initializing the first processor; determining whether the first processor is designated to operate in the active mode or the backup mode (column 5, lines 51-54 and column 6, lines 25-27); responsive to the first processor being designated to operate in the active mode, performing an active mode boot process (column 6, lines 56-60); responsive to the first processor being designated to operate in the backup mode, performing a backup mode boot process (column 6, lines 41-44); and performing system host functions (column 7, lines 2-6). Although Hammersley does not expressly disclose the step of "initializing the processor," this feature is deemed to be inherent (*see* definition for "boot (1)" as described in *The Authoritative Dictionary of IEEE Standards Terms*, 7th Edition, p. 113).

With regard to claims 7, 16, and 25, Hammersley discloses the method, system, and machine-readable medium, where transferring control of the first bus to the second processor includes the steps of: suspending control of and disconnecting the first processor from the first bus (column 6, lines 41-44); sending a switch-over message to

the second processor (column 5, lines 56-59 and column 6, lines 44-50); and activating device drivers on the second processor to take control of bus devices (column 5, lines 33-40 and column 6, lines 56-60).

Therefore, Hammersley reads on the invention as claimed.

Claim Rejections - 35 USC § 103

9. Claims 1 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,112,271 to Lanus, et al. ("Lanus") in view of *Structured Computer Organization*, 3rd Edition by Andrew S. Tanenbaum ("Tanenbaum).

With regard to independent claims 1 and 10, Lanus discloses a method and system (Fig. 1), where the method includes the steps of: operating a first processor (Fig. 1, item 150) connected with a first bus (Fig. 1, item 110) and a second bus (Fig. 1, item 120) wherein the first processor controls the first bus; operating a second processor (Fig. 1, item 170) connected with the first bus and the second bus wherein the second processor controls the second bus; detecting faults (column 5, lines 24-34); and responsive to an occurrence of a fault in the first processor, transferring control of the first bus to the second processor (column 5, lines 24-34).

Lanus does not expressly disclose detecting faults via hardware associated with the first processor and the second processor; transferring control of the first bus to the second processor via hardware associated with the first processor and the second processor; and where the hardware includes a Redundant Host Controller.

Tanenbaum discloses that hardware and software are logically equivalent (page 11, section 1.4), and therefore, any operation performed by software can be built directly into hardware. As such the software disclosed in Lanus functions as a redundant host controller, and this function can be built directly into hardware, as claimed.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine Tanenbaum with Lanus. The suggestion or motivation for doing so would have been to decrease cost and increase speed and reliability of the system.

Therefore, it would have been obvious to combine Tannenbaum with Lanus to obtain the invention as specified in claims 1 and 10.

Response to Arguments

10. Applicant's arguments, see pages 22-23, filed July 2, 2004, with respect to the rejections of claims 1 and 10 under 35 USC 102(b) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Tanenbaum.

The Examiner is persuaded that Lanus does not expressly disclose detecting faults via hardware associated with the first processor and the second processor; transferring control of the first bus to the second processor via hardware associated with the first processor and the second processor; and where the hardware includes a Redundant Host Controller.

However, Tanenbaum teaches that it would be obvious to use a hardware implementation for the detection of faults and transfer of control, as claimed.

11. Applicant's arguments filed July 2, 2004 with regard to the 35 USC 102(e) rejection in view of Hammersley have been fully considered but they are not persuasive.

The Examiner is not persuaded that Hammersley fails to teach using a redundant host controller to detect faults and transfer control. A controller is defined as a device that controls the transfer of data from a computer to a peripheral device and vice versa (*see* Webopedia definition for controller from www.webopedia.com). As described in column 5, lines 65-67 to column 6, lines 1-12, the disclosed I/O controller controls the transfer of data from a computer to associated peripheral devices. And as described in column 5, lines 41-44 and lines 61-64, and as shown in Fig. 2 (items 120, 122a, 122, and 120b), the controllers associated with the first and second are redundant.

Furthermore, Hammersley discloses detecting faults via hardware associated with the first processor and the second processor (column 6, lines 41-44). For example, the PCI controller 134b detects failure of the second processor unit, and the PCI controller 134b is a unit within the I/O controller 120(b). Hammersley also discloses transferring control of inoperative processors (column 6, lines 44-67 to column 7, lines 1-9). For example, the PCI controller 134b sends a signal to a hot swap controller 138b of the I/O controller 120b. In turn, the FET 146b is deactivated, and the PCI controller 134b is put into high impedance state to prevent the flow of I/O traffic through the primary controller 120b to or from the now failed second processor 110b.

Therefore, Hammersley reads on the invention as claimed.

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donna K. Mason whose telephone number is (571) 272-3629. The examiner can normally be reached on Monday - Friday, 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on (571) 272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DKM

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